Parallel Computing on SoC Architecture

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Outline

- Some history
- Modern Systems on Chip
- Computing on System on Chip, the INFN experience
- European Projects on low power computing
- Conclusion
Once upon a time....

The vector machines

Serial number 001 Cray-1™
- Los Alamos National Laboratory in 1976
- $8.8 million
- 80 MFLOPS scalar, 160/250 MFLOPS vector
- 1 Mword (64 bit) main memory
- 8 vector registers
  - 64 elements 64bit each
- Freon refrigerated
- 5.5 tons including the Freon refrigeration
- 115 kW of power
  - 330 kW with refrigeration

Serial number 003 was installed at the National Center for Atmospheric Research (NCAR) in 1977 and decommissioned in 1989


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Not properly wireless....
CRAY-XMP...Vector MultiProcessor

- 1982 CRAY-XMP 2 processors
  - 9.5 ns clock cycle (105 MHz)
  - 2x200 MFLOPS
  - 2M words (64 bit) = 16 MB

- 1984 CRAY-XMP four processors
  - 800 MFLOPS
  - 8M words
    - 64 MB main memory
  - about US$15 million
  - plus the cost of disks!!!
The Cray-2

- The Cray-2 released in 1985
- 4 processors
- 250MHz (4.1 ns)
- 256 Mword (64bit) Main Memory
  - 2 GByte
- 1.9 GFLOPS
- 150 - 200 kW
- Fluorinet cooling
- 16 sq ft floor space
- 5500 pounds
- About $17 million

The attack of the Killer Micros

Taken from the title of Eugene Brooks’ talk "Attack of the Killer Micros" at Supercomputing 1990

Caltech Cosmic Cube
- By Charles Seitz and Geoffrey Fox in 1981
- 64 Intel 8086/8087 processors
- 128 kB per processor
- 6 dimensions hypercube

(*)http://calteches.library.caltech.edu/3419/1/Cubism.pdf
The Killer Tomatoes

*Attack of the Killer Tomatoes* is a 1978 comedy horror film directed, produced, edited, scored and co-written by John DeBello.

Had three sequels!!!
Massively Parallel Processor (MPP)

- A single computer with many networked processors
  - Specialized interconnect networks
  - Low latency interconnection

- Up to thousands of processors

- Some examples
  - Connection Machines (CM-1/2/200/5)
  - Intel Paragon
  - ASCI series
  - IBM SP
  - IBM BlueGene
Thinking Machines

- 1985: Thinking Machines introduces the connection Machine CM-1

- Connection Machine CM-200
  - maximum configuration of 65536 1-bit CPUs(!)
  - floating-point unit for every 32 1-bit CPUs
  - A cube composed of 8 cubes
    - each cube contains up to 8096 processors
  - (The curved structure is a Data Vault - a disk array)
  - 40 GFLOPS peak

  - Featured in “Jurassic Park”

(*) Sources:
http://www.corestore.org/cm200.htm
http://en.wikipedia.org/wiki/Thinking_Machines_Corporation
Intel Paragon MPP

- Launched in 1993
- Up to 2048 (later 4000) Intel i860 RISC microprocessors
  - Connected in a 2D grid
  - Processors @ 50 MHz
- World most powerful supercomputer in 1994
  - Paragon XP/S140
  - 3680 processors
  - 184 GFLOPS peak

ASCI Red MPP

- 1996 At Sandia Laboratories
- Based on the Paragon architecture
- Fastest supercomputer from 1997 to 2000
  - 1.4 TFLOPS (peak) in 1997
  - 9152 cores
  - 3.2 TFLOPS (peak) in 1999
  - 9632 cores
- 1st supercomputer above 1 TFLOPS

IBM BlueGene/Q MPP

- **Trading the speed of processors for lower power consumption**
- System-on-a-chip design. All node components were embedded on one chip
- A large number of nodes
- 5D xTorus interconnect
- Compute chip is an 18 core chip
  - The 64-bit PowerPC A2
  - 4-way simultaneously multithreaded per core
  - 1.6 GHz
  - a 17th core for operating system functions
  - chip manufactured on IBM's copper SOI process at 45 nm.
  - 204.8 GFLOPS and 55 watts per processor
- Up to 20 PFLOPS (peak)
  - 16384 cores

Clusters

[a cluster is a] parallel computer system comprising an integrated collection of independent nodes, each of which is a system in its own right, capable of independent operation and derived from products developed and marketed for other stand-alone purposes.


- From “stack of Sparc Pizza Boxes” of the 80s to modern supercomputer

(*) Picture from: http://en.wikipedia.org/wiki/Computer_cluster
TOP500.org architectures share

ARCHITECTURES

(*) Source: http://s.top500.org/static/lists/2013/06/TOP500_201306_Poster.pdf
TOP500.org chip technology share

(*) Source: http://s.top500.org/static/lists/2013/06/TOP500_201306_Poster.pdf
Why did microprocessors take over?

- They have never been more powerful...
- …but they were cheaper, highly available and less power demanding

Cool people would say “greener”
Commodity hardware

- Microprocessors started to be mass produced and used in everyday life
  - Personal computer at home
  - Office automation
  - Gaming
What’s commodity nowadays?

Low-Power System on Chip (SoCs)

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Where do I find a SoC?

- Mobile
- Embedded
ARM based processor shipment

• ARM based processors are shipped in billions of units
• ARM licences the Intellectual Properties to manufactures
  • ...many manufactures ....
  • Samsung (Korea), MediaTek (China), Allwinner (China), Qualcomm (USA), NVIDIA (USA), RockChip (China), Freescale (USA), Texas Instruments (USA), HiSilicon (China), Xilinx (USA), Broadcom (USA), Apple (USA), Altera (USA), ST (EU), WanderMedia (Taiwan), Marvel (USA), AMD (USA) etc..
Vector vs Micro computing power

- CRAY-1
- HITACHI S820/60
- NEC SX-5
- NEC SX-ACE
- INTEL8086
- MOS 6510
- Pentium Pro
- INTEL i7
Vector vs Micro vs ARM based

Is history repeating?
Ok, but then....an iPhone cluster?

- **NO**, we are not thinking to build an iPhone cluster
- We want to use these processors in a standard computing center configuration
  - Rack mounted
  - Linux powered
  - Running scientific application mostly in a batch environment
- ..... Use development board...
ODROID-XU3

- Powered by ARM® big.LITTLE™ technology, with a Heterogeneous Multi-Processing (HMP) solution
  - 4 core ARM A15 + 4 cores ARM A7
- Exynos 5422 by Samsung
  - ~20 GFLOPS peak (32bit) single precision
- Mali-T628 MP6 GPU
  - ~110 GFLOPS peak single precision
- 2 GB RAM
- 2xUSB3.0, 2xUSB2.0, 1x107100 eth
- Ubuntu 14.4
- HDMI 1.4 port
- 64 GB flash storage

Power consumption max ~15 W
Costs 150 euro!

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Other nice boards

- WandBoard
- Rock2Board
- SabreBoard
- CubieBoard
- A80
- PandaBoard
- DragonBoard
- Texas Instruments EVMK2H

http://elinux.org/Development_Platforms

...and counting...

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### Some specs

<table>
<thead>
<tr>
<th>BOARD</th>
<th>Model</th>
<th>ARM IP</th>
<th>GPU IP</th>
<th>DSP IP</th>
<th>GFLOPS (CPU+GPU)</th>
<th>Eth</th>
</tr>
</thead>
<tbody>
<tr>
<td>FREESCALE (Embedded SoC) SABRE Board</td>
<td>Freescale i.MX6Q</td>
<td>ARM A9(4)</td>
<td>Vivante GC2100 (19.2GFlops)</td>
<td></td>
<td>25</td>
<td>1Gb</td>
</tr>
<tr>
<td>ARNDALE (Mobile SoC) Octa Board</td>
<td>Samsung Exynos 5420</td>
<td>ARM A15(4)</td>
<td>ARM Mali-T628 MP6 (110Gflops)</td>
<td>115</td>
<td>10/100</td>
<td></td>
</tr>
<tr>
<td>HARDKERNEL (Mobile SoC) Odroid-XU-E</td>
<td>Samsung Exynos 5410</td>
<td>ARM A15(4)</td>
<td>Imagination Technologies PowerVR SGX544MP3 (51.1 Gflops)</td>
<td>65</td>
<td>10/100</td>
<td></td>
</tr>
<tr>
<td>HARDKERNEL (Mobile SoC) Odroid-XU3</td>
<td>Samsung Exynos 5422</td>
<td>ARM A15(4)</td>
<td>ARM Mali-T628 MP6 (110 Gflops)</td>
<td>130</td>
<td>10/100</td>
<td></td>
</tr>
<tr>
<td>INTRINSIC (Mobile SoC) DragonBoard</td>
<td>Qualcomm Snapdragon 800</td>
<td>Qualcomm Krait(4)</td>
<td>Qualcomm Adreno 330 (130Gflops)</td>
<td>145</td>
<td>1Gb</td>
<td></td>
</tr>
<tr>
<td>TI (Embedded SoC) EVMK2H</td>
<td>TI Keystone 66AK2H14</td>
<td>ARM A15(2)</td>
<td></td>
<td></td>
<td>TMS320C66x (189Gflops)</td>
<td>1Gb (10Gb)</td>
</tr>
</tbody>
</table>

**TDP tra 5W e 15W (EVMK2H > 15W)**
How do you program them?? (in a Linux environment)

- GCC is available for ARM CPUs (for free)
- OpenCL for the GPU
  - If you are lucky enough to find working drivers
- Cross compilation
  - If you dare!
**NVIDIA JETSON K1**

- First **ARM + CUDA programmable** GPU-accelerated Linux development board!
- 4 cores ARM A15 CPU
- 192 cores NVIDIA GPU ➔ 300 GFLOPS (peak sp)
- ...for less than 200 Euros
Modern Accelerators

- Many simple cores to speed up parallel portions of code
  - GPUs for general purpose application
    - Available since mid 90s but now we have “reasonable” programming models
    - Intel XEON PHI (MIC ➔ Many Integrated Cores)

- High Performance/Watt ratio
  - (if properly used)
GPU acceleration in scientific computation

2 x (E5-2673v2 (IvyBridge) 8 cores)
~2 x 100 = 200 GFLOPS (double precision)
2 x 110 Watt = 220 W
~1 GFLOPS/W

1xNVIDIA TESLA K40
2880 cores
12 GB RAM
~1400 GFLOPS (double precision)
~4300 GFLOPS (single precision)
235 Watt
~6 GFLOPS/W dp
~18 GFLOPS/W sp

CPU+GPU ~ 3 GFLOPS/W dp
~ 9 GFLOPS/W sp
GPU acceleration in K1

4 core ARM A15 ~ 18 GFLOPS
Kepler SMX1 192 core ~ 300 GFLOPS

~ 15 Watt

~ 21 GFLOPS/W

N.B. Single precision – 32 bit architecture

~ 1.5 GFLOPS/€ (0.67 €/GFLOPS)
OK..good, that’s the theory...
...but what happens in reality?

- Real life is, as usual, harder than the theory
- In SOCs most of the power is in the GPU
- Extracting it could be unbelievably difficult
Limitations

Moreover commodity SoCs and development boards have a number of limitations:
- 32 bit
- Small caches
- Small RAM size
- No ECC memory
- Frequent failures and system crashes
- Slow connections in some cases
- HW bugs

*If anything can go wrong, it will.* (Murphy)
Not always perfect

![Graph showing throughput (Mbps) vs. data size (Bytes). The graph compares different network configurations: Xeon L5420 GigE, Sabreboard GigE (sender), and Sabreboard GigE (receiver).]
Prime numbers computation

CPU ONLY

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CMS@CERN results

CPU ONLY

High Energy Physics MonteCarlo simulations

Table 1. Results of run time tests for single core CMSSW (GEM-SIM) and a multi-threaded version of the Geant4 benchmark “FullCMS” with 4 threads (G4MT).

<table>
<thead>
<tr>
<th>Type</th>
<th>Cores</th>
<th>Power (TDP)</th>
<th>GEN-SIM Events/minute/core</th>
<th>GEN-SIM Events/minute/Watt</th>
<th>G4MT Events/minute (threads)</th>
<th>G4MT Events/minute/Watt</th>
</tr>
</thead>
<tbody>
<tr>
<td>ODROID U2</td>
<td>4</td>
<td>4W</td>
<td>1.08</td>
<td>1.08</td>
<td>34.2 (4)</td>
<td>8.6</td>
</tr>
<tr>
<td>ODROID XU+E</td>
<td>4/4</td>
<td>5W</td>
<td>1.47</td>
<td>1.07</td>
<td>47 (4)</td>
<td>9.4</td>
</tr>
<tr>
<td>dual Xeon <a href="mailto:L5520@2.27GHz">L5520@2.27GHz</a></td>
<td>2 x 4</td>
<td>120W</td>
<td>3.37</td>
<td>0.22</td>
<td>307.2 (16)</td>
<td>2.6</td>
</tr>
<tr>
<td>dual Xeon <a href="mailto:E5-2630L@2.0GHz">E5-2630L@2.0GHz</a></td>
<td>2 x 6</td>
<td>120W</td>
<td>3.46</td>
<td>0.35</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>


ARM slower by a factor 3 or 4 but...

...ARM better by a factor 3 or 5 on the power ratio
Molecular Dynamics on Jetson-K1

CPU+GPU

Parallel application for CPU and GPU

- Jetson-K1 about 10X slower using the same number of cores
- Jetson-K1 about 10X slower using the GPU (vs. an NVIDIA Tesla K20)
  - Jetson-K1 13.5Watt
  - Xeon+K20 ~320Watt

GROMACS use case

Lower is better
Lattice Boltzmann on the Tegra K1

GPU only

Lattice Boltzmann Methods: D2Q37

On Tegra-K1

15 GFLOPS
12 GB/s
$P_e \sim 10$Watt

40x slower than a K20m

LBM Performance Comparison (*)

<table>
<thead>
<tr>
<th></th>
<th>Xeon-Phi 7120</th>
<th>Tesla K20Xm</th>
<th>i7-4930K</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>OCL</td>
<td>C(*)</td>
<td>OCL</td>
</tr>
<tr>
<td>propagate T/iter [msec]</td>
<td>30.46</td>
<td>37.67</td>
<td>14.89</td>
</tr>
<tr>
<td>GB/s</td>
<td>76.42</td>
<td>61.8</td>
<td>156.33</td>
</tr>
<tr>
<td>$\epsilon_r$</td>
<td>22%</td>
<td>17%</td>
<td>62%</td>
</tr>
<tr>
<td>bc T/iter [msec]</td>
<td>3.20</td>
<td>4.61</td>
<td>7.08</td>
</tr>
<tr>
<td>collide T/iter [msec]</td>
<td>72.79</td>
<td>79.14</td>
<td>93.27</td>
</tr>
<tr>
<td>GFLOPS (DP)</td>
<td>410</td>
<td>377</td>
<td>320</td>
</tr>
<tr>
<td>MLUPS</td>
<td>54.02</td>
<td>49.69</td>
<td>42.16</td>
</tr>
<tr>
<td>$\epsilon_c$</td>
<td>34%</td>
<td>31%</td>
<td>24%</td>
</tr>
<tr>
<td>$\mu J$/site</td>
<td>5.55</td>
<td>6.03</td>
<td>5.57</td>
</tr>
<tr>
<td>$T_{WC}$/iter [msec]</td>
<td>106.45</td>
<td>121.42</td>
<td>115.24</td>
</tr>
<tr>
<td>MLUPS</td>
<td>36.94</td>
<td>32.38</td>
<td>34.12</td>
</tr>
</tbody>
</table>

(*) Schifano et al.; A portable OpenCL Lattice Boltzmann code for multi- and many-core processor architectures; Procedia Computer Science Volume 29, 2014, Pages 40-49, doi: 10.1016/j.procs.2014.05.004

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OK, nice...but...where is the cluster??

- We still need to build it
  - Waiting for a 64bit low cost, low power SoC

- INFN COSA project
  - Two years project starting in 2015
  - 50keuro per year
  - Build a 10 TFLOPS cluster with SoC architectures
  - **Prototype a scalable interconnect**
  - Test real life INFN parallel and scalar applications
Only ARM based SoCs?
And Intel?

- INTEL produce SoCs
  - Probably you have one in your laptop
- Some of them are low power
- Already 64bit
- Integrated GPU
  - CILK++ programmable
  - OpenCL programmable
### Some low power from Intel

<table>
<thead>
<tr>
<th>Nome prodotto</th>
<th>Intel Atom® Processor E8445 (2M Cache, 1.91 GHz)</th>
<th>Intel® Core™ M-5Y71 Processor (6M Cache, up to 2.90 GHz)</th>
<th>Intel® Core™ i7-4670U Processor (6M Cache, up to 3.60 GHz)</th>
<th>Intel® Core™ i7-4702EC Processor (6M Cache, up to 2.00 GHz)</th>
<th>Intel Atom® Processor C2730 (6M Cache, 1.70 GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nome in codice</td>
<td>Bay Trail</td>
<td>Broadwell</td>
<td>Haswell</td>
<td>Haswell</td>
<td>Avoton</td>
</tr>
<tr>
<td>Informazioni di base</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Stato</td>
<td>Launched</td>
<td>Launched</td>
<td>Launched</td>
<td>Launched</td>
<td>Launched</td>
</tr>
<tr>
<td>Data di lancio</td>
<td>Q4 '14</td>
<td>Q4 '14</td>
<td>Q3 '14</td>
<td>Q3 '14</td>
<td>Q3 '13</td>
</tr>
<tr>
<td>Numero di processore</td>
<td>E8445</td>
<td>5Y71</td>
<td>4670U</td>
<td>4702EC</td>
<td>C2730</td>
</tr>
<tr>
<td>Cache</td>
<td>2 MB L2 Cache</td>
<td>4 MB</td>
<td>4 MB</td>
<td>8 MB Intel® Smart Cache</td>
<td>4 MB</td>
</tr>
<tr>
<td>Set di istruzioni</td>
<td>64-bit</td>
<td>64-bit</td>
<td>64-bit</td>
<td>64-bit</td>
<td>64-bit</td>
</tr>
<tr>
<td>Opzioni integrate disponibili</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Litografia</td>
<td>22 nm</td>
<td>14 nm</td>
<td>22 nm</td>
<td>22 nm</td>
<td>22 nm</td>
</tr>
<tr>
<td>Prezzo consigliato per il cliente</td>
<td>TRAY: $52.00</td>
<td>TRAY: $291.00</td>
<td>TRAY: $428.00</td>
<td>TRAY: $459.00</td>
<td>TRAY: $150.00</td>
</tr>
<tr>
<td>Datasheet</td>
<td>Link</td>
<td>Link</td>
<td>Link</td>
<td>Link</td>
<td>Link</td>
</tr>
<tr>
<td>Privi di minerali provenienti da zone di conflitto</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Estensioni set di istruzioni</td>
<td>AVX, SSE</td>
<td>SSE 4.1/4.2, AVX 2.0</td>
<td>SSE 4.1/4.2, AVX 2.0</td>
<td>SSE 4.1/4.2, AVX 2.0</td>
<td></td>
</tr>
<tr>
<td>Tipo di bus</td>
<td>DM12</td>
<td>DM</td>
<td>DM</td>
<td>DM</td>
<td></td>
</tr>
<tr>
<td>Bus di sistema</td>
<td>5 GT/s</td>
<td>5 GT/s</td>
<td>5 GT/s</td>
<td>5 GT/s</td>
<td></td>
</tr>
<tr>
<td>Prestazioni</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Numero di core</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>4</td>
<td>8</td>
</tr>
<tr>
<td>Numero di thread</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Frequenza base del processore</td>
<td>1.91 GHz</td>
<td>2.90 GHz</td>
<td>3 GHz</td>
<td>2 GHz</td>
<td>17 GHz</td>
</tr>
<tr>
<td>TDP</td>
<td>10 W</td>
<td>4.5 W</td>
<td>28 W</td>
<td>27 W</td>
<td>12 W</td>
</tr>
<tr>
<td>Specifiche della grafica</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequenza di base grafica</td>
<td>542 MHz</td>
<td>300 MHz</td>
<td>200 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequenza di burst della grafica</td>
<td>792 MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Intel® Quick Sync Video</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Numero massimo di schermi supportati</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequenza dinamica massima grafica</td>
<td>600 MHz</td>
<td>1.2 GHz</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
2 cores + GPU
- Intel HD Graphics
- OpenCL 2.0 Support

4.5 Watt (TDP)

(*) http://www.notebookcheck.net/Intel-Core-M-5Y70-Broadwell-Review.130930.0.html

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Test on Intel AVOTON

N.B. - Preliminary results
N.B. - Old Xeon CPU

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European leadership?

- Mobile CPU and GPU (IP licenses)
  - ARM
  - Imagination Technology (iPhone GPU, MIPS tech)

- Embedded/Automotive/Avionics
  - Siemens
  - Bosch
  - ST
  - Infineon
The MontBlanc Project - 1

BSC ARM-based prototype roadmap

Prototypes are critical to accelerate software development
- System software stack + applications

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The MontBlanc Project - 2

- 15 node-cluster in a standard Bull B505 enclosure

- 6 BullX chassis
- 54 Compute blades
- 810 Compute cards
  - 1620 CPU
  - 810 GPU
  - 3.2 TB of DRAM
  - 52 TB of Flash

- 26 TFLOPS
- 18 kWatt
Data Centres (DCs) are a key resource for innovation and leadership of industry in Europe. They drive the Information Society through hosted cloud applications. To sustain the ever-increasing demand of storing and processing data, DCs need to improve their capabilities and scale in size. With current server technology, however, DC scaling is limited by the IT equipment’s density and energy consumption. To keep up with data growth, in the face of power distribution constraints and steadily increasing energy costs, the IT equipment must become dramatically smaller and more efficient in power and energy. This moves the focus of server design and the interests of industry from performance to power/energy efficiency and total cost of ownership (TCO).

The basic components of future servers and their integration into a full system must be reconsidered from the ground up. The processor, the memory hierarchy, I/O, the system interconnects and the systems’ software all require fundamental changes to match the application’s performance in less space and with drastically lower energy costs.

EUROSERVER is addressing these challenges in a holistic manner; we advocate the use of state-of-the-art low-power ARM processors in a new server system-architecture that uses 3D integration to scale with both the numbers of cores, and the memory and I/O, all managed by new systems software providing transparent system-wide virtualization and efficient resource use by cloud applications. The EUROSERVER prototype will demonstrate how the proposed approach can lead to 10x DC Energy Efficiency by 2020.
EU Horizon 2020 Call

ICT4 - Customised and low power computing

What we ask for (1)

Servers, micro-server and highly parallel embedded computing systems based on ultra-low power architectures

- Integration of HW and SW into working prototypes
- Low-power, low-cost, high-density, secure, reliable, scalable

Cross-layer programming approaches to exploit the full potential of heterogeneous parallel architectures

- Multi-dimensional optimisation (performance, energy, response time...)
- Programming approach per application class, easy for programmers
- Scalable market approach
The road to ExaScale

- A machine capable of running a parallel application (not embarassingly parallel) requiring $10^{18}$ fp operation per seconds
- A group of 1000 PetaScale machines is not an Exascale system

General agreed requirements
- available by 2018/2020
- Need less than 20 Mwatt

Need a factor 30 in the computing performance keeping the same power consumption of today machines
- Low power needed!

But....will exist in 2020 a parallel application requiring $10^{18}$ fp operation per seconds?
- There will be someone able to code it?

“And what comes after exascale? We can look forward to zettascale ($10^{21}$) and yottascale ($10^{24}$)….. Then we run out of prefixes.” (from: http://www.kurzweilai.net/designing-the-exascale-computers-of-the-future)
Conclusion

- The power consumption is becoming a key factor
  - From mobile systems...
  - ...to ExaScale supercomputers

- Mobile and embedded low power System-on-Chip are becoming attractive for scientific computing
  - Europe can play an industrial leadership role
  - European Commission is investing on it

- But they still have many limitations
  - Don’t just look at specs and GFLOPS count!!!

- The future is heterogeneous
  - A single system will have multiple type of processors
    - CPU, GPU, DSP, MIC....
  - Often in the same chip